

IN SITU SERIES CONNECTION FOR MULTI-JUNCTION THIN FILM CELLS

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ABSTRACT: To successfully compete with other photovoltaic technologies, amorphous silicon (aSi) based thin film modules have to increase their efficiency, but still reduce production cost. For higher efficiency, stacked cells are mandatory. For reducing cost, roll-to-roll deposition of flexible modules seems promising. This contribution presents the in situ series connection (ISSC) to combine several advantages of thin film technology into one manufacturing process. Successful wire patterning of aSi and ZnO proves the concept of ISSC for batch processing and web coating. Depending on the particular layer stack of tandem cells containing amorphous as well as microcrystalline doped silicon layers, the total loss F of ISSC ranges from $F = 5\%$ to $F = 12\%$. An outlook on the transfer of ISSC to industrial web coating concludes the paper.

Keywords: a-Si:H, multijunction, module, flexible, monolithic, series connection

1 INTRODUCTION

Shortly after Carlson and Wronski [1] reported the first amorphous silicon (aSi) solar cell in 1976, Hamakawa [2] presented first multi-junction cells with an output voltage up to 2.4 V and a power conversion efficiency $\eta = 4\%$ of a stack of four aSi cells with identical absorber bandgap but optimized absorber thicknesses. During the past 30 years several research groups and companies developed aSi based cell stacks with various concepts. Since many years, triple junction stacks employing absorber layers of different bandgaps achieve the best performance. Yang et al. [3] reported an initial efficiency $\eta = 14.6\%$ for a triple-junction cell with the middle and bottom cells containing SiGe alloys.

The world market share of aSi based photovoltaic (PV) modules was below 5% in recent years, competing with a similar, but rapidly rising share of CdTe thin film modules and with the advanced technologies of screen printing crystalline silicon (cSi) wafers at high production yield and throughput. Therefore PV technologies based upon aSi and microcrystalline Si (μcSi) must meet the targets of system cost set by the 90% market share of the screen-printed cSi modules.

Besides processing Si thin films on very large area glass plates [4], roll-to-roll manufacturing [5,6] is a promising alternative for meeting the cost targets. For implementing monolithic series connection, polymer foil substrates facilitate the electric isolation of neighbouring cell stripes [7], in contrast to metal foil [5], but need further improvement of the efficiency of flexible tandem cells over the recently reported $\eta = 9\%$ at $T < 180^\circ\text{C}$ [8]. Reviewing the current status of aSi based PV technologies indicates various promising features. Unfortunately, up to now none of the technologies combines all the advantages into one joint concept.

This contribution therefore pursues to combine the main advantages of aSi based PV technologies into one single processing scheme. The key for reaching this goal is the in situ series connection (ISSC) which implements the monolithic series connection on slightly bent substrates by wire shading and shifting during thin film deposition [9,10]. Single-junction aSi modules on polyethylene-naphthalate (PEN) foil with $\eta = 3.3\%$ and a total

interconnection loss $F = 15\%$ prove the ISSC concept [11]. This contribution extends the application of ISSC to tandem cell structures and investigates the resulting interconnection losses for two prototype layer stacks with suitable wire shift sequences.

The use of wire masking instead of laser scribing allows to reduce the total interconnection loss of modules based on tandem cells to $F < 5\%$, not only on flexible foil, but also on rigid glass substrates. Large-area glass substrates sag due to gravity when mounted face down. The resulting curvature is large enough to enable patterning of all constituent layers of the cell structure [9]. Alternatively, substrate carriers can enforce an appropriate bending of rigid substrates, such as glass, metal or plastic sheets. Hence, ISSC is feasible for batch or inline processing of rigid glass plates as well as for web coating of low-cost plastic foil.

High performance Si thin film modules consist of stacked cells in order to reduce cost by raising the cell efficiency. In contrast to laser scribing, which generally cuts the complete layer stack, wire shading opens a wealth of possible combinations of wire shift and layer deposition sequences for optimizing the module performance. This paper only discusses two prototype examples, namely a 2-shift sequence suited for amorphous doped layers, and a 4-shift sequence optimized for microcrystalline doped layers.

Finally we present first experimental results on the wire patterning of aSi and of ZnO:Al in a reel-to-reel cassette manufactured by MVSystems [12] which enables further testing and optimization of the ISSC for single- and multi-junction based PV modules.

2 WIRE PATTERNING

The ISSC technology masks the substrate during thin film deposition with stainless steel wires or other filaments. To implement monolithic series connection of single cell stripes into a PV module, the deposition sequence of the multi-junction devices includes a number of wire shifts.

In order to ensure reliable patterning during plasma enhanced chemical vapour deposition (PECVD) and sputtering, the substrate has to be slightly bent.

Therefore the first proof of concept of ISSC employed PEN foil [11]. Moreover, recent investigations of the quality and reliability of wire patterning for ISSC revealed that the inevitable sagging of common large-area glass substrates enables ISSC on rigid substrates as well [9]. Even glass plates of 1 mm thickness and $10 \times 5 \text{ cm}^2$ size easily bend to a curvature radius $r_b > 900 \text{ mm}$, which allows us to perform ISSC experiments on glass on laboratory scale.

Figure 1a presents the schematic view of a simple experimental setup for evaluating the ISSC. The wire assembly is manually lifted and shifted during vacuum breaks between the thin film deposition steps. Further details on feasibility studies performed with a $15 \times 15 \text{ cm}^2$ substrate carrier are reported in refs. [9-11].

Figures 1b and 1c show exemplary results of the wire patterning during sputter deposition of aluminium doped zinc oxide ZnO:Al with single wires of $100 \mu\text{m}$ diameter (Fig. 1b), and with two closely adjacent wires of $50 \mu\text{m}$ diameter (Fig. 1c). The 3D micrographs of Figs. 1b and 1c have been recorded with a Keyence VK-9700 confocal laserscan microscope that provides a resolution of 1 nm in the direction perpendicular to the layer surface. Both patterning schemes provide complete electrical separation of the low resistive transparent conductive oxide (TCO) stripes.

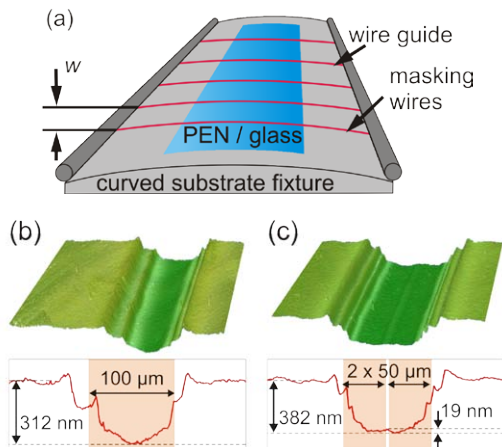


Figure 1: Wire patterning for in-situ series connection. a) ISSC substrate holder for batch processing of modules on rigid glass or on plastic foil. Wire guides position the wires and allow for small wire shifts. b) 3D mapping with Keyence VK-9700 confocal laserscan microscope of sputtered ZnO:Al on glass isolated with stainless steel wires of $d_w = 100 \mu\text{m}$. c) ZnO:Al separation with three times higher reliability by double-wire shading with $d_w = 50 \mu\text{m}$; no deposition occurs between wires.

Compared with single-wire patterning in Fig. 1b, the more rectangular cross section of Fig. 1c enhances the reliability of the patterning. Two adjacent wires give a double chance for isolating neighbouring stripes without lateral short circuits. Even if a patterning line is interrupted due to e.g. dust particles, those will hardly affect the very same position across both wires. Moreover, there is almost no deposition in-between the wires since plasma ignition is suppressed due to the very close spacing of the wires.

Very similar to the results on ZnO patterning in Figs. 1b and 1c, detailed investigations of the wire shading of aSi PECVD prove perfect separation down to a wire diameter of $100 \mu\text{m}$ [9]. Compared with ZnO sputtering, the wire shading of aSi or μcSi PECVD benefits even more from the suppression of plasma formation in-between two adjacent wires of $50 \mu\text{m}$ diameter.

3 SERIES CONNECTION OF STACKED CELLS

Figure 2 depicts a cross section of an aSi-based thin film PV module including the monolithic series connection of its tandem cell stripes in a superstrate configuration, i.e. with the sun light entering through the transparent superstrate at the bottom. The initial position of the masking wires separates the sputtered ZnO:Al front contact into stripes which extend perpendicular to the plane of drawing. After the first wire shift of distance w_s , the masking wire inhibits the deposition of the *pin-pin* layer stack onto the shaded ZnO:Al underneath the wire, and thereby enables later access to the front contact.

Due to the asymmetry of charge carrier transport, the light must enter aSi and μcSi based *pin* cells through the *p*-type doped layer. Hence the common superstrate configuration depicted in Fig. 2 requires to deposit the top cell first. In our example, a second wire shift opens access to the front contact after the *pin* deposition of the bottom cell is completed. Eventually, monolithic series connection forms during the sputtering of a thin TCO mirror layer and a metal back contact on top of the layer sequence depicted in Fig. 2.

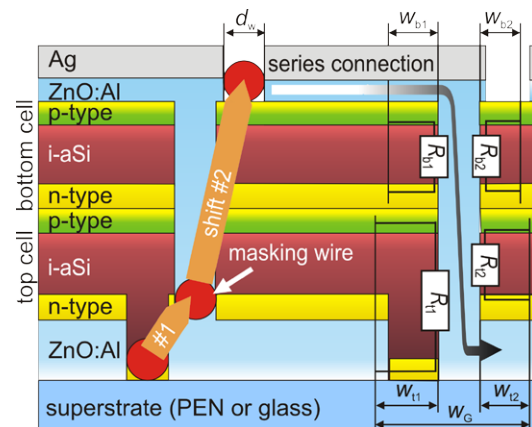


Figure 2: Superstrate tandem cells with monolithic series connection by ISSC. Initial masking wire position isolates the front contacts, shift #1 masks the front contact during *pin-pin* cell deposition. Shift #2 opens access to the front contact for series connection during ZnO:Al mirror and Ag deposition and isolates the back contacts. The doping layers of the *pin-pin* structure induce shunting paths at the top and bottom cells, but those affect the performance of the cells only within the widths w_{t1} , w_{t2} , w_{b1} , w_{b2} . For aSi doping layers the shunts are negligible the total interconnection loss drops below 5%.

The total interconnection loss F due to the monolithic series connection depicted in Fig. 2 includes a loss of active area due to the patterning lines, and resistive losses due to voltage drops across the top ZnO stripes

along the path of the module current. The following considerations present some simple approximations which allow for estimating the loss contributions and their dependence on layer properties and various wire shift sequences.

The p -type window layer of the top cell in Fig. 2 has a conductivity $\sigma_{p,top}$ and thickness $d_{p,top}$. The inner p - n tunnel junction between the top and bottom cells forms a sheet resistance $r_{in} = (\rho_{n,in} \rho_{p,in}) / (\rho_{n,in} d_{p,in} + \rho_{p,in} d_{n,in})$, deduced from the resistivities $\rho_{n,in}$ and $\rho_{p,in}$ of the inner n - and p -type layers with thicknesses $d_{n,in}$ and $d_{p,in}$.

The following loss calculations assume an additional 'electrically dead area' at the edges of the cell stripes, in addition to the dead area needed for the mere geometrical separation of the cell stripes, and the resistive ZnO loss. The indicated distances w_{t1} , w_{t2} , w_{b1} , and w_{b2} describe an effective loss of active module area due to shunts introduced by the interconnection, close to the edges of the cell stripes. Those distances represent positions in the single cells where the lateral voltage drop across the parasitic resistances equals the cell voltage at maximum power output V_{MPP} .

In general, the interconnection induces different shunt paths at the left-hand and at the right-hand sides of the cell stripes in Fig. 2. The shunt paths R_{t1} and R_{b2} are either negligible for amorphous doped layers, or easily removed by performing the wire shifts #1 before depositing the top cell p -type, and #2 before the bottom cell n -type layers [11]. The remaining $R_{t2} = r_{in} L w_{t2}$ in top cells, and $R_{b1} = r_{in} L w_{b1}$ in bottom cells effectively decrease the cell widths by w_{t2} and by w_{b1} . As a most simple approximation, we consider the cell performance homogeneous and unaffected over the active width $w_{act} = w - w_G$ of the cell stripes where no patterning lines cause parasitic shunts or dead area. The gap width $w_G = d_w + w_{t1} + w_{b2}$ for $w_{t1} > w_s$ and $w_{b2} > w_s$ or $w_G = d_w + 2 w_s$ for $w_{t1} < w_s$ and $w_{b2} < w_s$ results from the interconnection gap and the parasitic shunt losses. The distances w_{t2} and w_{b2} define the 'electrically dead area' which collects parasitic shunt current. For quantifying w_{t2} and w_{b2} , we follow the calculation of Gupta [13] to determine voltage drops $V_{t2} = r_{in} J (w_{t2})^2 / 2$ and $V_{b1} = r_{in} J (w_{b1})^2 / 2$ which balance the MPP voltages of the respective cells $V_{t2}(w_{t2}) = V_{MPP,t}$ and $V_{b1}(w_{b1}) = V_{MPP,b}$ at those positions. We assume typical MPP parameters of well optimized tandem cells $V_{MPP,b} = 0.5$ V and $V_{MPP,t} = 0.8$ V with a current matching at $J = 8$ mA cm⁻².

If the inner tunnel junction only consists of amorphous doped layers with $\rho_{n,aSi} = 10^3$ Ωcm and $\rho_{p,aSi} = 10^4$ Ωcm, the resulting $w_{t2} = 5$ μm and $w_{b1} = 4$ μm are very narrow. Hence the effectively shunted area is much smaller than the dead area due to front and back contact masking, rendering the shunts R_{t2} and R_{b1} negligible. For an all amorphous inner tunnel junction, the very simple configuration of Fig. 2 yields total interconnection losses as low as $F = 5$ %, including resistive TCO loss.

In contrast, if both doped layers of the inner tunnel junction consist of μcSi, the total width of the effectively shunted area is $w_G = d_w + w_{t2} + w_{b2} = 2.25$ mm with $w_{t1} = 1.2$ mm and $w_{b2} = 950$ μm. In this case the geometrical area loss due to d_w is negligible. The dead area of width

w_{dead} leads to a lower limit $F = 17$ % for an optimum wire distance $w_w = 18.8$ mm (see Fig. 1).

For the most realistic case of an aSi/μcSi tunnel junction obviously two configurations exist. The combination n -μcSi/ p -aSi causes similar losses $F = 17$ % as before, due to the low $\rho_{n,\mu cSi}$. The use of p -μcSi/ n -aSi reduces total loss to $F = 13.5$ % for $w_w = 16.3$ mm.

Since $F > 13.5$ % is too high for successfully implementing ISSC, Figure 3 proposes an advanced wire-shifting sequence to reduce the total loss of ISSC for tandem cells. Our feasibility study uses a wire frame according to Fig. 1a and adds two wire shifts #2 and #3, while #1 and #4 correspond to the two shifts of Fig. 2, optimized according to [11]. Thus the shunt path R_{t1} of Fig. 2 is removed. Preliminary experiments prove that the corresponding introduction of the p - n tunnel junction into the low ohmic top-to-bottom interconnection of neighbouring cell stripes does not hamper its performance.

The wire shifts #2 before, and #3 after the deposition of the inner tunnel junction isolate the top cell against the interconnection gap, thereby reducing total losses to $F = 12$ % at $w_w = 15.1$ mm, re-optimized for an all μcSi inner tunnel junction, and to $F = 10$ % at $w_w = 13.6$ mm for a n -aSi/ p -μcSi tunnel junction.

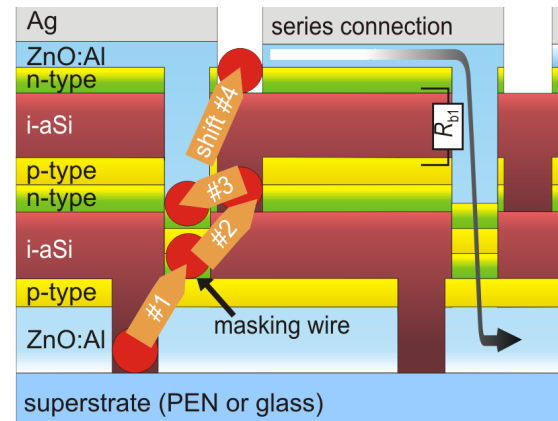


Figure 3: Improved wire shift sequence for μcSi doping layers. Shift #1 after ZnO and p -μcSi avoids R_{t1} , shift #2 before and #3 after inner doping layer deposition isolate R_{t2} . Shift #4 before p -type deposition removes R_{b2} . R_{b1} still limits the total interconnection loss to $F = 12$ % for a p -μcSi/ n -μcSi tunnel junction, or to $F = 10$ % for a n -aSi/ p -μcSi one.

4 ROLL-TO-ROLL PROCESSING

Silicon thin film modules composed of stacked solar cells on the one hand significantly gain in stabilized efficiency over their single-junction predecessors and thereby improve competitiveness with other PV technologies, but on the other hand cause higher cost and manufacturing effort.

Roll-to-roll deposition of flexible thin film modules with inline series connection by ISSC instead of laser scribing opens a pathway towards cost reduction in mass production. Although not addressed here, one has to keep in mind that encapsulation cost of flexible modules must come down significantly in order to compete with large area glass based thin film PV.

Taking a first step, our feasibility studies pursue to demonstrate aSi based ISSC modules from roll-to-roll processing at a small laboratory scale.

Figure 4 presents a reel-to-reel cassette designed for roll-to-roll deposition of flexible ISSC modules in a PECVD cluster tool [12]. A novel wire frame and a slightly curved backing plate of the cassette enable wire shading for ISSC. Batch processing in a cluster tool with separate chambers for *p*-type, *n*-type and intrinsic Si layers decouples the optimization of the single layers and easily avoids cross contaminations which need special care in industrial web coaters. The wire frame supports precise positioning and shifting of the complete wire assembly, but needs a vacuum break for manual operation. More advanced future setups will incorporate automated wire shifting.

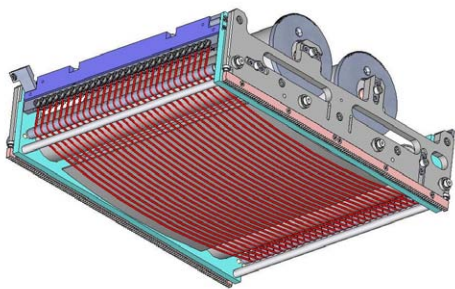


Figure 4: Reel-to-reel cassette for testing dynamic deposition of ISSC modules in a PECVD cluster tool. A feed and a take-up roll drive the substrate through the deposition area. The wire frame precisely positions and shifts the masking wires for patterning single layers.

Figure 5 shows first undoped aSi film deposition on PEN foil with the reel-to-reel cassette modified for ISSC. The periodical bright lines indicate the patterning lines. Sputter deposition of ZnO:Al proves the successful electrical separation of neighbouring stripes by wire shading.

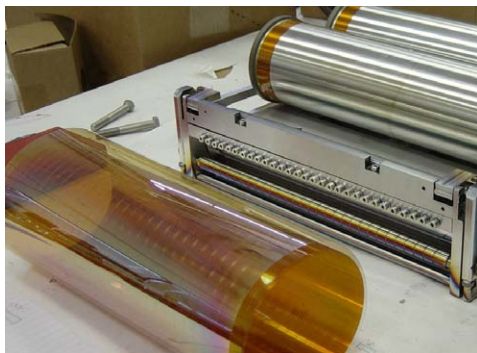


Figure 5: First aSi films patterned by wire shading during roll-to-roll deposition on a 30 cm wide PEN foil with the reel-to-reel cassette seen in the background.

Figure 6 gives an outlook on transferring the ISSC technology, which is currently tested in batch processing, to an inline roll-to-roll manufacturing without the need of breaking the vacuum for wire shifts.

Inline processing with fixed masking wire positions enables individual patterning configurations for each single layer. Thereby the remaining shunt path R_{b2} of Fig. 3 can be removed to further lower the total intercon-

nection loss down to $F = 4.9\%$ at an optimum cell width of $w_w = 9.2$ mm, when assuming similar MPP tandem cell performance as for the loss calculations given above.

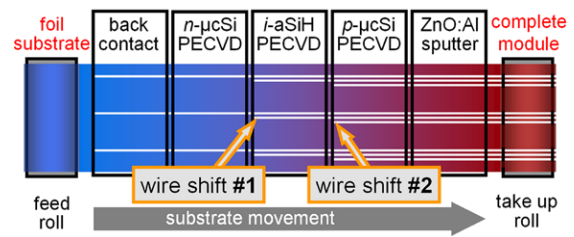


Figure 6: ISSC for inline roll-to-roll processing. Instead of wire shifts, the masking wires directly mount into the different chambers at fixed offsets of the wire positions.

5 CONCLUSION

The in situ series connection ISSC replaces laser scribing for monolithic series connection and opens a low-cost route to the roll-to-roll manufacturing of flexible thin film PV modules. First steps of our feasibility study demonstrate that the ISSC of stacked thin film cells enables total interconnection losses below 10 % for batch processing, while for advanced inline processing the lower limit on total loss drops below 5 % .

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